REMARKS

Claims 3, 5-8 and 11-22 have been examiner in the present application. Claims 3, 5-8 and 11-16 have been allowed. Claims 17-20 are rejected under 35 U.S.C § 102(e) over Matsuoka (U.S. Pat. No. US 2004/0037107). Claims 21 and 22 have been objected to. Claim 17 has been cancelled and claims 18, 19 and 21 have been amended hereby. In light of the above amendments and below remarks, reconsideration of the present application is respectfully requested.

Applicants gratefully acknowledge the allowance of claims 3, 5-8 and 11-16. Claims 21 and 22 were objected to as being dependent upon a rejected base claim, but were indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants defer rewriting claims 21 and 22 until final resolution of the rejected claims.

In paragraph 2 of the Office Action, claims 17-20 are rejected under 35 U.S.C § 102(e) over Matsuoka. Applicants respectfully traverse this rejection. Claim 17 has been cancelled. Claim 18 has been rewritten to include all of the limitations of claim 17. Claim 19 and 21 were rewritten to depend on claim 18.

Amended claim 18 explicitly requires "a second column decoder receiving **and using** a portion of a row address signal." (emphasis added). Applicants respectfully submit that this feature of the present invention is neither taught nor suggested by Matsuoka.

In rejecting the above-mentioned limitation of claim 18, the Office Action relied on Figure 7 of Matsuoka pointing to elements 252A and 252B. In contrast to the systems illustrated in Figures 1 and 10 of Matsuoka, the system of Figure 7 does not include control circuits 153A and 153B. It is unclear from the description in Matsuoka

whether the omission of these control circuits in Figure 7 is merely an oversight or was intentional. Regardless, claim 18 as amended explicitly requires that the second column decoder receives and actually uses a portion of a row address signal. Even if it was intentional that Matsuoka did not include control circuit 153a in the circuit of Figure 7, Applicants respectfully submit that Matsuoka fails to teach or suggest that the second column decoder actually uses a portion of the received row address signal as recited in claim 18.

At best, one skilled in the art would assume that the decoders 252 in Figure 7 of Matsuoka strip away the addresses that are not used for it's operation. For example, the column decoders 252 strip away the row addresses and the row decoders 251 similarly strip away the column address. There is no description whatsoever in Matsuoka that the column decoder 252 actually uses a portion of the row address that it may receive. Viewing Figure 7 in conjunction with Figs. 1 and 10, one skilled in the art would simply be motivated to include the functionality of control circuits 153 in decoders, namely, supplying column addresses in the column decoders and row addresses in the row decoders. Again, Matsuoka is completely silent with respect to actually using a portion of the row address in a column decoder as required by claim 18 and one skilled in the art would not have any suggestion or motivation to make such a modification to Matsuoka.

For at least this reason, amended claim 18 is patentable over Matsuoka.

Claims 19 and 21 are dependent on claim 18 and include all of its limitation. Therefore, all of the above arguments made in favor of claim 18 apply equally to claims 19 and 21. Withdrawal of the rejection of claims 18, 19 and 21 is respectfully requested

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By _____
Ian R. Blum
Registration No.: 42,336
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
1177 Avenue of the Americas
41st Floor
New York, New York 10036-2714
(212) 835-1400
Attorney for Applicant